

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method for improving amplifier efficiency, comprising:
providing a power mode signal to change a power level at which the amplifier is operating;
providing an amplifier load circuit responsive to the power mode signal, wherein a high impedance is presented in a low power mode and a low impedance is presented in a high power mode;
correcting signal distortion in a high power mode of the amplifier with at least one linearizing module, wherein the power amplifier, while operating in at least one low power mode, is substantially unaffected by the at least one linearizing module; and
reducing a signal component with at least one power mode-based signal shaping module.
2. (previously presented) The method of claim 1, wherein the at least one linearizing module is selected from a group comprising a phase shift circuit responsive to the power mode signal, a predistortion linearizer, a switchable predistortion linearizer, a dual harmonic resonance filter, a harmonic resonance filter, and a switch responsive to the power mode signal providing a connection to one or more of a ground, a supply terminal and a reference terminal.
3. (original) The method of claim 2, wherein the switchable predistortion linearizer is a switchable cubic predistortion linearizer.
4. (original) The method of claim 2, wherein a switch responsive to the power mode signal isolates the amplifier from the at least one linearizing module.
5. (previously presented) The method of claim 1, wherein the at least one

power mode-based signal shaping module is selected from a group comprising one or more of a phase shift circuit responsive to the power mode signal, a predistortion linearizer, a switchable predistortion linearizer, a dual harmonic resonance filter, a harmonic resonance filter, and a switch responsive to the power mode signal providing a connection to one or more of a ground, a supply terminal and a reference terminal.

6. (original) The method of claim 1, wherein the at least one linearizing module also reduces a signal component.
7. (original) The method of claim 5, wherein one or more frequency spurs are reduced by the at least one power mode-based signal shaping module in a power mode selected from a high power mode and a low power mode.
8. (original) The method of claim 7, wherein a high impedance is presented during one or more of operation in a low power mode and at a fundamental frequency by the at least one power mode-based signal shaping module.
9. (original) The method of claim 5, wherein a phase is adjusted by the at least one power mode-based signal shaping module in a power mode selected from a high power mode and a low power mode.
10. (original) The method of claim 1, wherein the power mode signal has a value in a low power mode of about 0V and in a high power mode of about 3V.
11. (previously presented) The method of claim 2, wherein the dual resonance harmonic filter comprises a first filter inductor and a filter capacitor connected in parallel and both the first filter inductor and the filter capacitor are in series with a second filter inductor with a ratio between inductances of the first filter inductor and the second filter inductor of about three to one.
12. (currently amended) A power amplifier circuit with improved efficiency, comprising:
a power amplifier load circuit responsive to a power mode signal, ~~wherein~~

including at least one switch responsive to the power mode signal couples a signal processed by coupled between an output of the power amplifier circuit to and a ground node;
a switchable cubic predistortion linearizer coupled to an input of the power amplifier and responsive to the power mode signal, and
a bias circuit including a dual resonance harmonic filter coupled between a supply node and at least one stage in the power amplifier.

13. (original) The power amplifier circuit with improved efficiency in accordance with claim 12, further comprising a capacitor and a switch responsive to a band select signal connected to one another in series between a node in the power amplifier load circuit and the ground.

14 – 17. (canceled)

18. (currently amended) A method of providing multiple power modes in a power amplifier circuit, the method comprising:
providing a phase shift circuit responsive to a power mode signal at an input of the power amplifier circuit;
providing a dual resonance harmonic filter in a bias circuit for biasing at least one stage in the power amplifier circuit while presenting a low impedance to a harmonic of a fundamental frequency and a high impedance to the fundamental frequency; and
providing a load circuit responsive to the power mode signal to provide a suitable impedance in a lower power mode to improve efficiency in the lower power mode.

19. (currently amended) The method of claim 18 further comprising providing a switchable cubic predistortion linearizer that is invoked during high power amplification by the power amplifier circuit.

20. (original) The method of claim 18 further comprising providing at least two serially connected amplifier stages, each biased by a corresponding current mirror

responsive to the power mode signal.

21. (currently amended) A method of providing multiple power modes in a power amplifier circuit, the method comprising:
providing means for phase shifting in response to a power mode signal at an input of the power amplifier circuit;
providing filtering means in a bias circuit for biasing at least one stage in the power amplifier circuit, wherein the filtering means present a low impedance to a harmonic of a fundamental frequency and a high impedance to the fundamental frequency; and
providing loading means responsive to the power mode signal to provide a higher impedance in a lower power mode.
22. (currently amended) The method of claim 21 further comprising providing predistortion means that are invoked in response to the power mode signal during high power amplification by the power amplifier circuit.
23. (previously presented) The method of claim 21 further comprising providing at least two serially connected amplifier stages, each biased by a corresponding current means that are responsive to the power mode signal.